REMARKS

Applicant is in receipt of the Office Action mailed December 18, 2002. Claim 21 was rejected under Section 112, and claims 1 – 33 were rejected under Section 103.

Section 112 Rejection

Claim 21 was rejected under Section 112 because there was insufficient antecedent basis for the term "said second parallel bus". Applicant has amended claim 21 to correct the antecedent basis error.

Section 103 Rejection

Applicant notes the Summary of the Invention at page 5, beginning at line 3, which recites as follows:

> A PCI bus cycle includes an address phase and one or more data phases. The address phase further includes a command value and an address value, and each data phase further includes a set of byte enable values and a data value. The PCI bus cycle can be received by either a primary or secondary bridge. When the primary or secondary bridge accepts a PCI bus cycle, it stores the information contained in the address phase and in each data phase into a queue. The bridge then generates a series of packets that correspond to the stored PCI bus cycle when the address phase of the PCI bus cycle reaches the head of the queue. The series of packets includes a command packet and a plurality of data packets. The bridge then transmits the series of packets over the serial bus to the other respective bridge.
>
> The bridge first generates a command packet as part of the series of packets. A command packet includes a set of predicted byte enable values. The set of actual byte enable values is not known until the data phase reaches the head of the queue. When the data phase reaches the head of the queue, the set of actual byte enable values is compared with the set of predicted byte enable values included in the command packet. If the set of actual byte enable values matches the set of predicted byte enable values, then the primary bridge continues to generate packets for the address value and the data value or values. If the set of actual byte enable values differs from the set of predicted byte enable values, then the primary bridge generates another command packet that includes the set of actual byte enable values and discards the earlier command packet. Thus,

if the predicted byte enable values match the actual byte enable values, then the bridge generates packets with increased efficiency. If the predicted byte enable values are later determined to be incorrect when the actual byte enable values arrive at the head of the queue, then the bridge generates a second command packet at that time, which is when the bridge would otherwise be required to generate the command packet. Thus, the present invention provides improved performance for a large number of cycles.

Thus, one embodiment of the invention involves generation of a "set of predicted byte enable values". As noted above, when the data portion of the transfer is available, the set of actual byte enable values is compared with the set of predicted byte enable values included in the command packet. If the set of predicted byte enable values matches the set of actual byte enable values, then the already generated command packet including the predicted set is used. This increases the efficiency of the transfer.

As amended, claim 1 recites in part:

> wherein said primary bridge is configured to generate a first command packet that corresponds to said address phase, wherein said primary bridge is configured to generate a plurality of data packets that each correspond to said parallel bus cycle, wherein said first command packet includes a second set of byte enable values, and wherein said primary bridge is configured to set said second set of byte enable values to a set of predetermined values prior to generating said plurality of data packets, wherein said predetermined values comprise predicted values of the first set of byte enable values.

Thus the "predetermined values" in claim 1 above refer to predicted values of the byte enable values. In a similar manner, the various other independent claims recite the notion of "predetermined" byte enable values or "predicted" byte enable values.

The cited references do not teach or suggest the notion of predicted (or predetermined) byte enable values. The Office Action evidently relies on the Baker reference as teaching this limitation, stating that it is "well known to predetermine or predict the size of the data bursts that are about to be transmitted" (citing cols. 13-16, and esp. Table 1 of Baker). Applicant has reviewed the Baker reference, and in particular the cited portions mentioned above, and cannot find any mention of generation of predicted byte enable signals. More specifically, Table 1 of Baker mentions the concept of byte

enable signals, but does not teach or suggest the notion of predicting byte enable values prior to knowing what the "actual" byte enable values will be. Applicant submits that the cited reference does not teach or suggest the notion of "predicted values" or setting of "predetermined values" of byte enable signals as recited in the present claims.

Applicant also notes that the Baker reference is directed generally to "an information processing system". Applicant submits that there is no teaching or suggestion to combine the references as proposed by the Examiner.

Thus, Applicant submits that independent claims 1, 11, 22, and 34, and those dependent thereon, are allowable. Applicant further submits that the various dependent claims are independently allowable.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Conley, Rose, & Tayon, P.C. Deposit Account No. 50-1505/5150-30300/JCH.

Also enclosed herewith are the following items:

☒ Return Receipt Postcard

☐ Request for Approval of Drawing Changes

☐ Notice of Change of Address

☐ Check in the amount of $ for fees ( ).

☐ Other:

Respectfully submitted,

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